REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

In the specification, paragraph **[0002]** has been amended.

Claim 5 is currently being amended.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier. Paragraph **[0002]** has been amended to update serial number assignments. Claim 5 has been amended to correct a clerical error.

After amending the claims as set forth above, claims 1-31 are now pending in this application.

I. Claim Rejections under 35 U.S.C. § 101

On page 2 of the Office Action, in section 1, the Examiner rejected claims 1-6, 30 and 31 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The Examiner argues that: "Claims 1 and 30 constitutes abstract ideas and therefore is a judicial exception and not statutory subject matter. [sic] Also the abstract ideas are not used in a practical application to provide a useful, concrete, and tangible result." Applicants respectfully traverse the rejection. The Examiner has not followed Federal Circuit precedent. The § 101 requirements for patentable subject matter are to be construed liberally:

> The repetitive use of the expansive term "any" in § 101 shows Congress's intent not to place any restrictions on the subject matter for which a patent may be obtained beyond those specifically recited in § 101. Indeed, the Supreme Court has acknowledged that Congress intended § 101 to extend to "anything under the sun that is made by man." … Thus, it is improper to read limitations into § 101 on the subject matter that may be patented where the legislative history indicates that Congress clearly did not intend such limitations.

State St. Bank & Trust Co. v. Signature Fin. Group, 149 F.3d 1368, 1373 (Fed. Cir. 1998).

"[T]he Court has held that mathematical algorithms are not patentable subject matter to the extent that they are merely abstract ideas." *Id.* However, the Court has consistently held that a method is not abstract where *any* useful, concrete and tangible result can be identified:

> Unpatentable mathematical algorithms are identifiable by showing they are merely abstract ideas constituting disembodied concepts or truths that are not "useful." From a practical standpoint, this means that to be patentable an algorithm must be applied in a "useful" way. In Alappat, we held that data, transformed by a machine through a series of mathematical calculations to produce a smooth waveform display on a rasterizer monitor, constituted a practical application of an abstract idea (a mathematical algorithm, formula, or calculation), because it produced "a useful, concrete and tangible result"--the smooth waveform.
>
> Similarly, in Arrhythmia Research Technology Inc. v. Corazonix Corp.,…, we held that the transformation of electrocardiograph signals from a patient's heartbeat by a machine through a series of mathematical calculations constituted a practical application of an abstract idea (a mathematical algorithm, formula, or calculation), because it corresponded to a useful, concrete or tangible thing--the condition of a patient's heart.

Id. (underlining added).

In the present application, Applicants have claimed methods which have useful, concrete, and tangible results. Claim 1 is directed to "demodulation of a composite signal containing a plurality of multi-path components." Claim 30 is directed to "demodulating a CDMA-compliant waveform." Clearly, "demodulation of a composite signal" and "demodulating a CDMA-compliant waveform" relate to useful, concrete, and tangible results. Applicants have met the standard set by the Guidelines on Subject Matter Eligibility published in O.G. 11/22/2005 and incorporated into the MPEP sections 2106-2106.02 8th edition, Rev. 5, August 2006. Demodulation is specific, substantial, and credible (i.e., "useful"). It is reproducible and a result can be assured (i.e., "concrete"). It provides a "real world" result (i.e., "tangible").

As Applicants have satisfied requirements of subject matter eligibility and in view of the liberal interpretation of § 101, Applicants respectfully request withdrawal of the rejection of claims 1 and 30 for at least the above reasons.

Additionally, the Examiner argues that: "Claims 2-6 and 31 are rejected as incorporating the deficiency of claims 1 and 30 upon which they depend." For at least the above reasons, Applicants respectfully request withdrawal of the rejection of claims 2-6 and 31.

II. Claim rejections under 35 U.S.C. § 102(e)

1. Claims 1-4 and 6

On pages 2-4 of the Office Action, in section 3, the Examiner rejected claims 1-4, and 6 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,985,516, Easton et al. (hereafter "Easton"). The Examiner argues that:

> [a]s shown in figures 2 and 5, Easton discloses a method for demodulation of a composite signal containing a plurality of multi-path components, the method comprising: … randomly accessing the digital samples from the first memory element to correlate a particular multi-path component from the signal (block 522 in figure 5); and iteratively accumulating the correlated particular multi-path component into a second memory element (blocks 524, 526, and 234 in figure 5).

Applicants respectfully traverse the rejection. Further, Applicants reserve the right to swear behind Easton as a prior art reference.

a. Easton does not randomly access digital samples from a memory

Easton does not teach, disclose, or suggest "randomly accessing the digital samples from the first memory element to correlate a particular multi-path component from the signal." In the Office Action, to support the position that Easton includes in this claim element, the Examiner cites block 522 in figure 5. The text in the specification related to the operation of block 522 (the "correlator") is found in column 12, lines 21-35. Also, the text describing Figure 7A describes a specific embodiment of the correlator. (column 18, lines 1-11.) Both of these cites in Easton merely describe standard PN despreading. Neither of these operational descriptions teach, disclose, or suggest "randomly accessing the digital samples from the first memory" as required by Claim 1. Futher, Applicants reserve the right to swear behind Easton as a prior art reference.

b. Easton does not iteratively accumulate

Furthermore, Easton does not teach, disclose, or suggest "iteratively accumulating the correlated particular multi-path component into a second memory element." The Examiner cites blocks 524, 526, and 234 in figure 5. Applicants respectfully traverse the rejection.

In the present application, "iteratively accumulating," refers to the methods overviewed in Figure 3 and described in part by Figures 6 and 9. Importantly, "iteratively" modifies "accumulating" to show that more than standard accumulation is taking place; otherwise, the modifier "iteratively" would be superfluous. In part, "iteratively accumulating" captures that the accumulation is not necessarily occurring in a continuous or periodic manner as shown in Figure 3. Paragraph **[0041]** provides an overview of Figure 3:

> FIG. 3 illustrates operation of the processor 20 compared to operation of a conventional synchronous implementation. Whereas the conventional implementation operates continuously and relatively uniformly on incoming chips, the processor 20 does the required amount of processing at the fastest clock rate available in a serial fashion. This speed enables the processor 20 to finish its processing before the time needed for the next buffer to fill and require servicing (i.e., a Symbol Group Duration). The processor 20 can be shut down (i.e., the clock is gated off) until the completion of the Symbol Group Duration. As also shown in FIG. 3 by the width of block sections, the given amount of processing may vary from Symbol Group to Symbol Group.

(underlining added.) Easton does not teach, disclose, or suggest "iteratively accumulating" as it is described in the present application and required by claim 1. In Easton, blocks 524 (symbol demodulator and combiner), 526 (accumulator), and 234 (buffer/de-interleaver) merely represent the functional equivalents of what was known in the art at the time. Easton does not operate these elements in an iterative accumulating operation.

An anticipatory rejection cannot be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, Applicants respectfully request withdrawal of the rejection of claim 1. Furthermore, Applicants respectfully traverse the arguments posed by the Examiner relative to claims 2-6 as these claims are allowable for at least the reasons

outlined above relative to claim 1. Therefore, Applicants respectfully request withdrawal of the rejection of claims 1-6.

2. Claims 30-31

On page 4 of the Office Action, in section 4, the Examiner rejected claims 30 and 31 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication 2004/0165567 Kim et al. (hereafter "Kim"). The Examiner argues that:

> …with regard to claim 30, [a]s shown in figures 3-7, Kim discloses a method of processing data based on programmed instructions, the method comprising: demodulating a CDMA-compliant waveform, wherein the CDMA-compliant waveform is processed asynchronously to a sample rate associated with the waveform during processing of communication chips and based on programmed instructions in programmed memory (see figures 3-7, page 1, paragraphs [0013]).

Applicants respectfully traverse the rejection. Further, Applicants reserve the right to swear behind Kim as a prior art reference. Further, Applicants hereby reserve the right to argue that some matter in the 26 August 2004 publication of Kim cannot be used as § 102(e) prior art. Applicants note that the applications from which Kim claims priority do not have the same named inventors in each application. Applicants reserve the right to swear behind Kim and any of its parent applications as prior art references.

a. Kim does not process asynchronously

Kim does not teach, disclose, or suggest "demodulating … wherein the CDMA-compliant waveform is processed asynchronously to a sample rate associated with the waveform during processing of communication chips and based on programmed instructions in programmed memory." Paragraph **[0013]** of Kim, referring to Figures 3 and 4, discloses "[a] system block diagram of a prior art linear multiuser detector for synchronous or asynchronous CDMA communication … ." Kim is simply describing that his system may be used in an Asynchronous CDMA network scheme; not that "the CDMA-compliant waveform is processed asynchronously to a sample rate." Further, Figures 3 -7 do not show "process[ing] asynchronously to a sample rate." Moreover, is should be noted that Kim is directed to spreading codes, not "demodulation of a composite signal containing a plurality of multi-path components". (*See* Boesel Abstract; Boesel Para. **[0040]**) Therefore, Kim does not teach, disclose, or

suggest "[a] method of processing data based on programmed instructions, the method comprising: demodulating a CDMA-compliant waveform, wherein the CDMA-compliant waveform is processed asynchronously to a sample rate associated with the waveform during processing of communication chips and based on programmed instructions in programmed memory."

An anticipatory rejection cannot be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, Applicants respectfully request withdrawal of the rejection of claim 30. Furthermore, Applicants respectfully traverse the arguments posed by the Examiner relative to claim 31 as this claim is allowable for at least the reasons outlined above relative to claim 30. Therefore, Applicants respectfully request withdrawal of the rejection of claims 30 and 31.

III. Claim rejections under 35 U.S.C. § 103

On page 5 of the Office Action, in section 6, the Examiner rejected claims 5, 7-8, 11-12, 15-25 and 28-29 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of U.S. Patent No. 6,853,839, Usuda et al. (hereafter "Usuda"). On page 11 of the Office Action, in section 7, the Examiner rejected claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda and further in view of U.S. Patent Application Publication No. 2002/0176489, Sriram et al. (hereafter "Sriram"). On page 12 of the Office Action, in section 8, the Examiner rejected claims 13 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda and further in view of U.S. Patent Application Publication No. 2002/0094017, Wang (hereafter "Wang"). On page 13 of the Office Action, in section 9, the Examiner rejected claims 26 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda and further in view of U.S. Patent No. 6,795,489, Joshi et al. (hereafter "Joshi"). Applicants respectfully traverse the rejections.

1. Claim 5

a. Easton does not disclose all recited elements

On page 5 of the Office Action, in section 6, the Examiner rejected claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda. As shown above, claim 5 should be allowed for at least the reasons outlined above relative to claim 1 since an obviousness rejection cannot

be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, for at least this reason, Applicants respectfully request withdrawal of the rejection of claim 5.

b. Usuda does not perform channel estimation and demodulation via the non-sequential access of digital samples

With regard to claim 5, the Examiner argues that: "Usuda teaches performing channel estimation via the non-sequential access of digital samples (see block 303 in figure 3)."

Applicants respectfully traverse the rejection. Neither Usuda nor Easton teach, disclose, or suggest "performing channel estimation and demodulation via the non-sequential access of digital samples form the first memory element." "Block 303" of Figure 3 in Usuda is a standard channel estimator; there is nothing remarkable about the channel estimator of Usuda anywhere in the specification. The Examiner cites Usuda Col. 3, lines 36-39 to support her argument. *In fact, the text that follows the Examiner's cite* ***teaches away*** *from the claimed features*: "operating the instantaneous estimation for estimating the antenna weights … in parallel with the accumulative estimation for demodulating the received data." (underlining added) (Col. 3, lines 39-42.) Hence, Easton in view of Usuda does not teach, disclose, or suggest "performing channel estimation and demodulation via the non-sequential access of digital samples form the first memory element" as required by claim 5.

An obviousness rejection cannot be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, for at least the above reasons, Applicants respectfully request withdrawal of the rejection of claim 5.

2. Claims 7-19

On page 5 of the Office Action, in section 6, the Examiner rejected claims 7-8, 11-12, 15-19 under 35 U.S.C. § 103 as being unpatentable over Easton in view of Usuda. On page 11 of the Office Action, in section 7, the Examiner rejected claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda and further in view of Sriram. On page 12 of the Office Action, in section 8, the Examiner rejected claims 13 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda and further in view of Wang. Applicants respectfully traverse

the rejections and hereafter argue that allowance of claim 7 and its dependent claims should be granted for at least the following reasons with respect to Easton and Usuda.

a. Easton and Usuda do not operate via random access

With regard to claim 7, the Examiner argues that: "[a]s shown in figures 2 and 5, Easton discloses an apparatus configured to demodulate a composite signal containing a plurality of multi-path components, the apparatus comprising: … a despreading element that operates via random access of buffers that are currently in read state to accumulate energy for a particular multi-path component." The Examiner cites column 12, lines 24-29 of Easton.

Applicants respectfully traverse the rejection. Neither Usuda nor Easton teach, disclose, or suggest "a despreading element that operates via random access of buffers that are currently in read state to accumulate energy for a particular multi-path component." Column 12, lines 24-29 merely describes standard PN despreading which was well known in the art at the time.

Hence, Easton in view of Usuda does not teach, disclose, or suggest "a despreading element that operates via random access of buffers that are currently in read state to accumulate energy for a particular multi-path component." as required by claim 7.

b. Easton and Usuda do not iteratively accumulate

Furthermore, neither Easton nor Usuda teach, disclose, or suggest "an accumulator that iteratively accumulates the despread energy for each particular multi-path component into a buffer." The Examiner cites blocks 524 and 526 in figure 5. Applicants respectfully traverse the rejection.

In the present application, "iteratively accumulating," refers to the methods overviewed in Figure 3 and described in part by Figures 6 and 9. Importantly, "iteratively" modifies "accumulating" to show that more than standard accumulation is taking place; otherwise, the modifier "iteratively" would be superfluous. Specifically, "iteratively accumulating" captures that the accumulation is not necessarily occurring in a continuous or periodic manner as shown in Figure 3. Paragraph **[0041]** provides an overview of Figure 3:

> FIG. 3 illustrates operation of the processor 20 compared to operation of a conventional synchronous implementation. Whereas the conventional implementation operates continuously and relatively uniformly on incoming chips, the processor 20 does the required amount of processing at the fastest clock rate available in a serial fashion. This speed enables the processor 20 to finish its processing before the time needed for the next buffer to fill and require servicing (i.e., a Symbol Group Duration). The processor 20 can be shut down (i.e., the clock is gated off) until the completion of the Symbol Group Duration. As also shown in FIG. 3 by the width of block sections, the given amount of processing may vary from Symbol Group to Symbol Group.

Easton does not teach, disclose, or suggest "an accumulator that iteratively accumulates the despread energy for each particular multi-path component into a buffer" as it is described in the present application and required by claim 7. Referring to Easton, blocks 524 (symbol demodulator and combiner) and 526 (accumulator) merely represent the functional equivalents of what was known in the art at the time. Easton does not operate these elements in anything other than a manner that was standard at the time.

An obviousness rejection cannot be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, for at least the above reasons, Applicants respectfully request withdrawal of the rejection of claim 7. Furthermore, Applicants respectfully traverse the arguments posed by the Examiner relative to claim 8, 11, 12, 15, 16, 17, 18, and 19 as these claims are allowable for at least the reasons outlined above relative to claim 7. Therefore, Applicants respectfully request withdrawal of the rejection of claims 7, 8, and 11-19.

Additionally, because the Examiner relies on Easton and Usuda in the rejection of claims 9-10 and 13-14, these claims are allowable for at least the above reasons. Therefore, Applicants respectfully request withdrawal of the rejection of claims 7-19.

3. Claim 8

Furthermore, with specific regard to claim 8, the Examiner argues that: "Easton further teaches a power control operable to power-down circuitry after the processing of all desired multi-path components and to power-up when the next buffer of sample data is ready to be processed." The examiner cites column 13, lines 45-59 of Easton which reads in relevant part: "[i]n an embodiment, a data write address

pointer is initialized to the designated address upon the occurrence of a reset event (e.g., power up)." Applicants respectfully traverse the rejection.

Easton does not teach, disclose, or suggest "power-up when the next buffer of sample data is ready to be processed." Column 13, lines 45-59 of Easton describe initialization of a system and a memory addressing scheme. This is in contrast to the present application where:

> During the *period of inactivity* between completion of processing and waiting for the sample buffer to synchronously fill (the shaded regions), the clock is disabled. This can be seen in FIG. 3 in the shaded "Shut Down" region. As a result, there is no idle power loss from the processor 20 due to capacitive loading on the clock tree resulting from clock ticks on the circuitry without activity. In conventional systems using an ASIC for demodulation operations, only a small fraction of the clock ticks produce useful output from the ASIC.

(underlining and emphasis added) (Para. **[0042]**.) The selective power-down of circuits, described and claimed in the present application, as quoted above, is distinguished from the initialization procedure described in Easton. Therefore, Easton does not teach, disclose, or suggest "a power control operable to power-down circuitry after the processing of all desired multi-path components and to power-up when the next buffer of sample data is ready to be processed" as required by claim 8.

An obviousness rejection cannot be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, for at least the above reasons, Applicants respectfully request withdrawal of the rejection of claim 8.

4. Claims 20-29

On page 9 of the Office Action, in section 6, the Examiner rejected claims 20-25 and 28–29 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda. On page 13 of the Office Action, in section 9, the Examiner rejected claims 26 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Easton in view of Usuda and further in view of Joshi. Applicants respectfully traverse the rejections and hereafter argue that allowance of claim 20 and its dependent claims should be granted for at least the following reasons with respect to Easton and Usuda.

a. Easton and Usuda do not operate via random access

With regard to claim 20, the Examiner argues that: "[a]s shown in figures 2 and 5, Easton discloses a demodulator operable with spread spectrum signals in a multi-path communication environment, the demodulator comprising: a despreader that obtains digital samples from a first memory buffer by randomly accessing the first memory buffer." The Examiner cites column 12, lines 23-30. Applicants respectfully traverse the rejection.

Neither Usuda nor Easton teach, disclose, or suggest "a despreader that obtains digital samples from a first memory buffer by randomly accessing the first memory buffer." Column 12, lines 23-30 of Easton merely describes standard PN despreading which was well known in the art at the time.

Hence, Easton in view of Usuda does not teach, disclose, or suggest "randomly accessing the first memory buffer." as required by claim 20.

b. Easton and Usuda do not adapt to arbitrary sample rates and symbol times

Furthermore, neither Easton nor Usuda teach, disclose, or suggest "a despreader …, whereby the despreader is adaptable to arbitrary sample rates and symbol times." The Examiner cites figures 2 and 5, and column 12, lines 23-30 of Easton. Applicants respectfully traverse the rejection.

Column 12, lines 23-30 of Easton merely describes standard PN despreading which was well known in the art at the time. In contrast, the present application describes that: "[a]dvantageously, sample buffers 22 make it possible for the processor 20 to not be synchronously clocked by the sample rate because the processor 20 can obtain data from sample buffers 22 as needed. (Para. **[0040]**.) Moreover, "[w]hereas the conventional implementation operates continuously and relatively uniformly on incoming chips, the processor 20 does the required amount of processing at the fastest clock rate available in a serial fashion. This speed enables the processor 20 to finish its processing before the time needed for the next buffer to fill and require servicing." (Para. **[0041]**.) Hence, "sample buffers 22 make it possible for the processor 20 to not be synchronously clocked by the sample rate because the processor 20 can obtain data from sample buffers 22 as needed." (Para. **[0040]**.) Another example of the dynamic processing ability of the processor 20 is the dynamic setting of bit-widths. (Para. **[0043]**.)

Easton does not teach, disclose, or suggest "[a] demodulator operable with spread spectrum signals in a multi-path communication environment, the demodulator comprising: a despreader that obtains digital samples from a first memory buffer by randomly accessing the first memory buffer, whereby the despreader is adaptable to arbitrary sample rates and symbol times," as required by claim 20.

An obviousness rejection cannot be properly maintained where the reference used in the rejection does not disclose all of the recited claim elements. Therefore, for at least the above reasons, Applicants respectfully request withdrawal of the rejection of claim 20. Furthermore, Applicants respectfully traverse the arguments posed by the Examiner relative to claim 21-25 and 28–29 as these claims are allowable for at least the reasons outlined above relative to claim 20. Therefore, Applicants respectfully request withdrawal of the rejection of claims 20-25 and 28–29.

Additionally, because the Examiner relies on Easton and Usuda in the rejection of claims 26 and 27, these claims are allowable for at least the above reasons. Therefore, Applicants respectfully request withdrawal of the rejection of claims 20-29.

Therefore Applicants respectfully request withdrawal of the rejection of claims 1-31 for at least the above reasons. Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant

hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date: July 12, 2007

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